



# **Technoprobe S.p.A. Mediobanca Mid Cap Conference 2026**

**January 22, 2026**



**TECHNOPROBE**



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# Innovation begins with us

A leading company in the field of semiconductors and microelectronics



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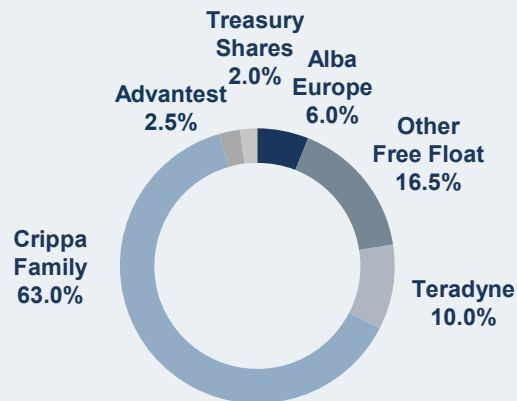


# Company Overview

## 2024 Key financial metrics

Revenue	Ebitda	Net Income	Net Financial Position	Mkt Cap
<b>€543.2m</b> <b>+22%</b> CAGR 19-24	<b>€136.5m</b> <b>25%</b> EBITDA margin	<b>€62.8m</b> <b>12%</b> on revenues	<b>€656.3m</b> as at 12/31/2024	<b>~€10,3bn</b> as at 1/21/2025

## Shareholding Structure



Leading player in designing and manufacturing of **probe cards to test Logic chips**



Manufacturing process **vertical integrated**



Strong focus on **innovation**



Extensive **global presence** and widespread **local footprint**



# Where we are

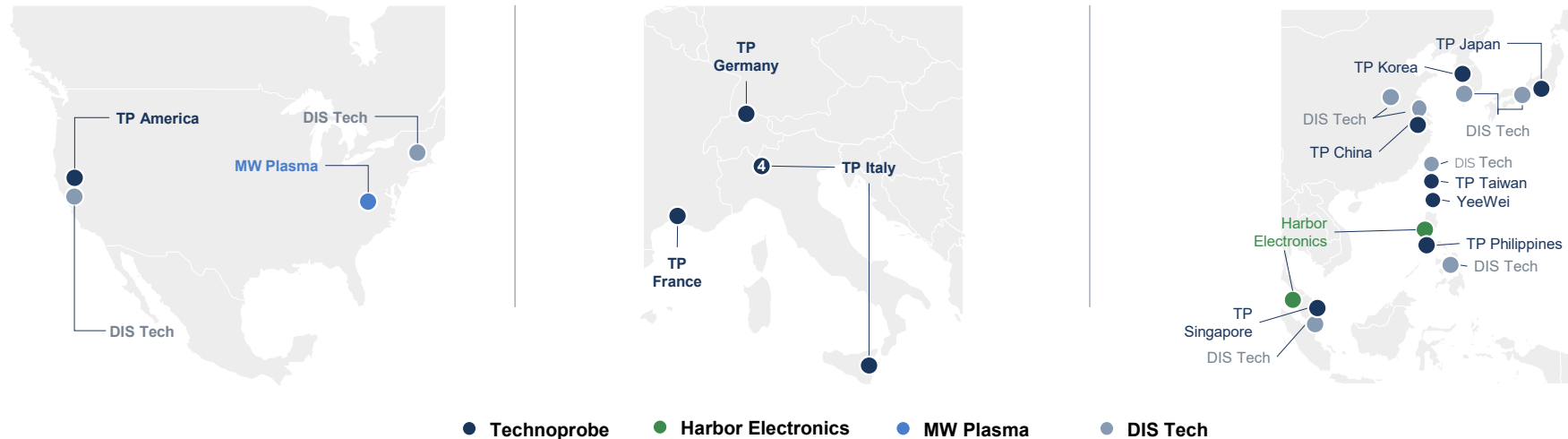
Headquartered in Italy with branches in Europe, America, and Asia

**>3.3k Employees**

**3 Continents**

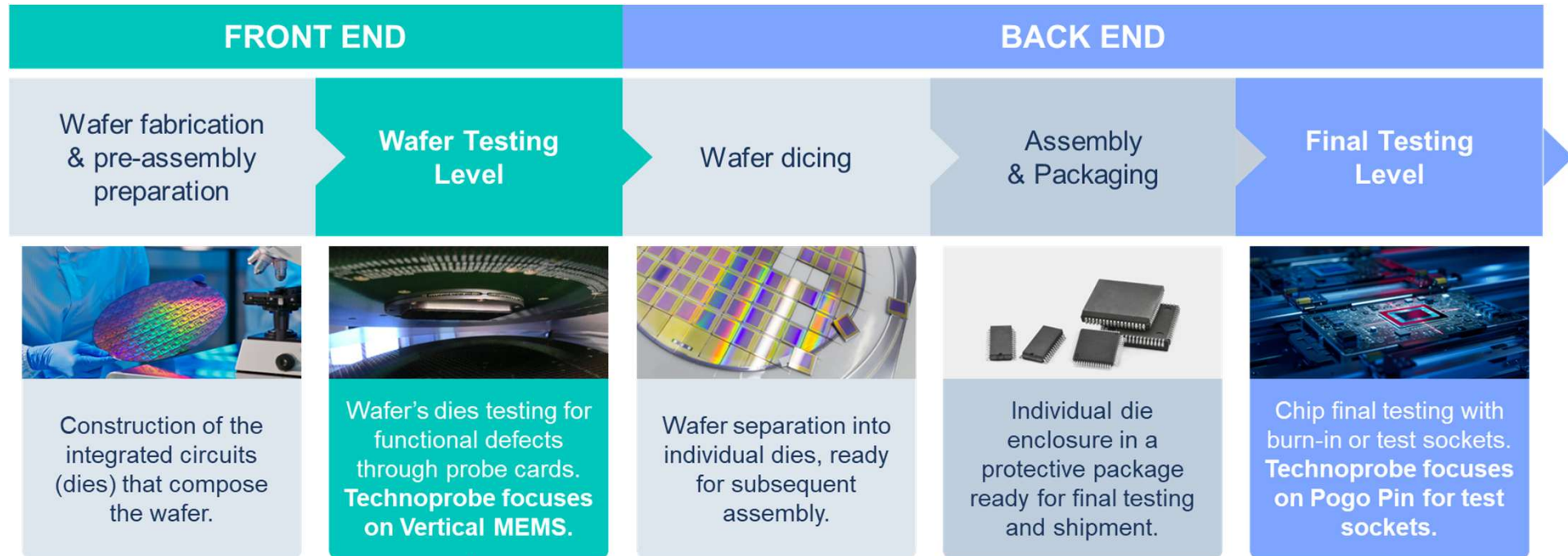
**10 Countries**

**23 Legal Entities**



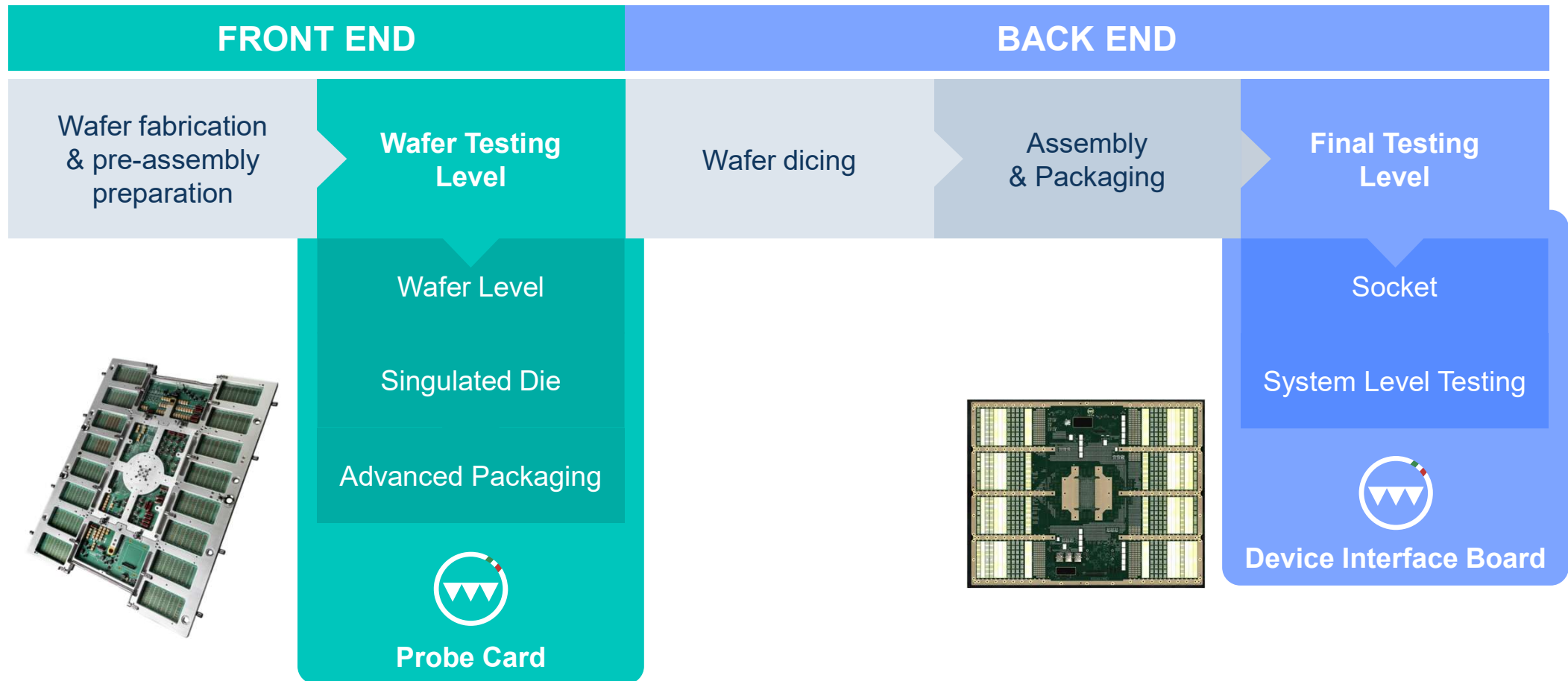


# Probe Cards in the semiconductor manufacturing process





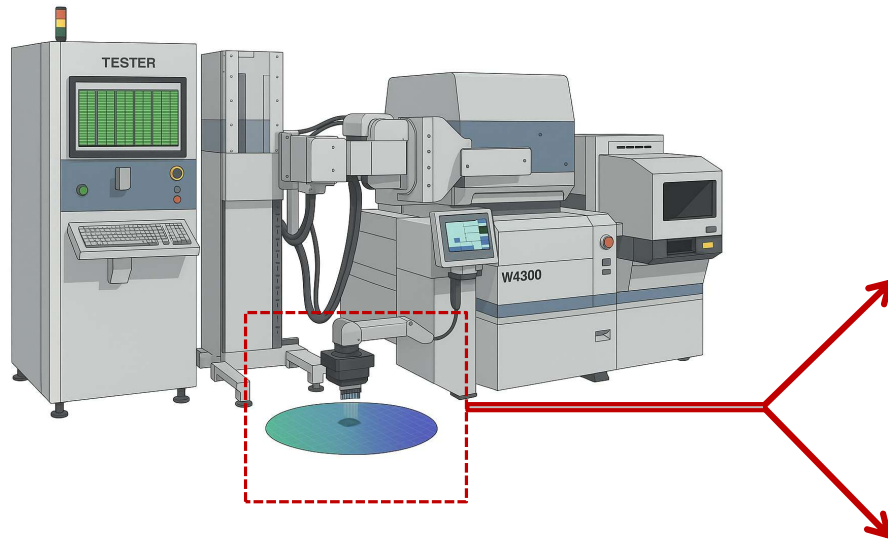
# Our positioning in the testing space







# The testing phase

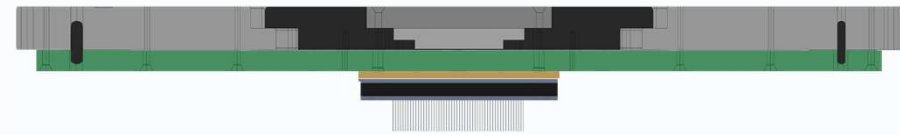


## Tester (ATE)

- A tester, or Automated Test Equipment (ATE), applies electrical signals to semiconductor devices and measures their responses to verify performance and functionality
- ATE systems execute test programs to identify manufacturing defects and ensure chips meet design specifications

## Probe Card

- A probe card is a precision device with microscopic needles or MEMS tips that make electrical contact with each die's test pads on the wafer
- The probe card connects the tester (ATE) to the wafer, enabling parallel testing of multiple dies before they are diced into individual chips



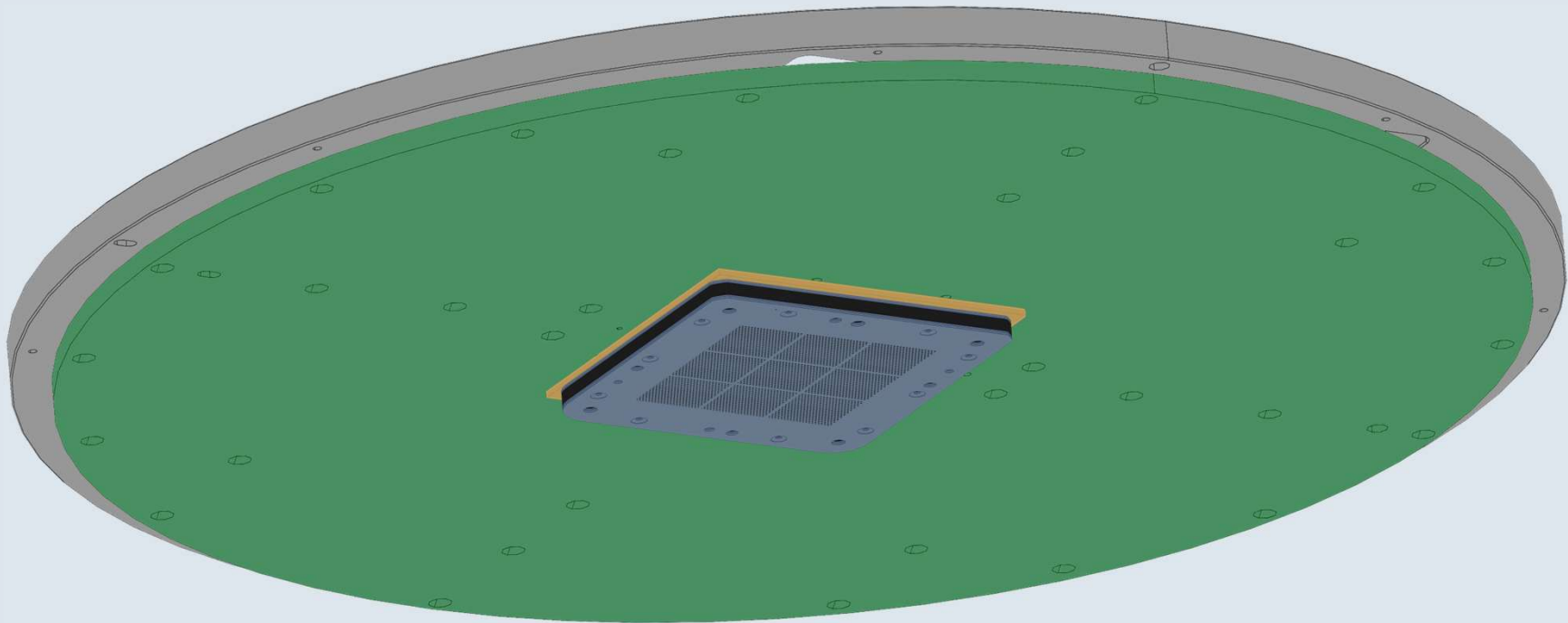
## Wafer

- A wafer is a thin, circular semiconductor substrate (most commonly silicon) on which integrated circuits (dies) are fabricated
- Each die functions as an individual integrated circuit that, once separated (diced) and packaged with external connectors, becomes a finished semiconductor chip



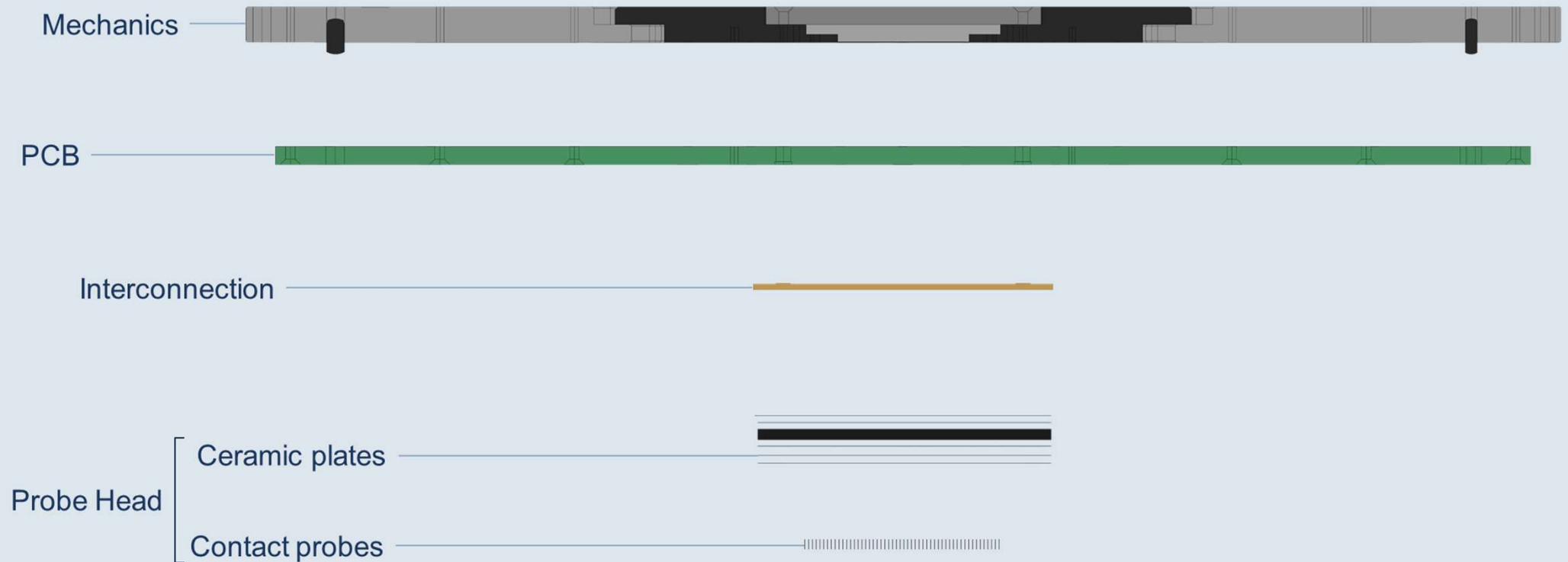


# The Probe Card





# The Probe Card





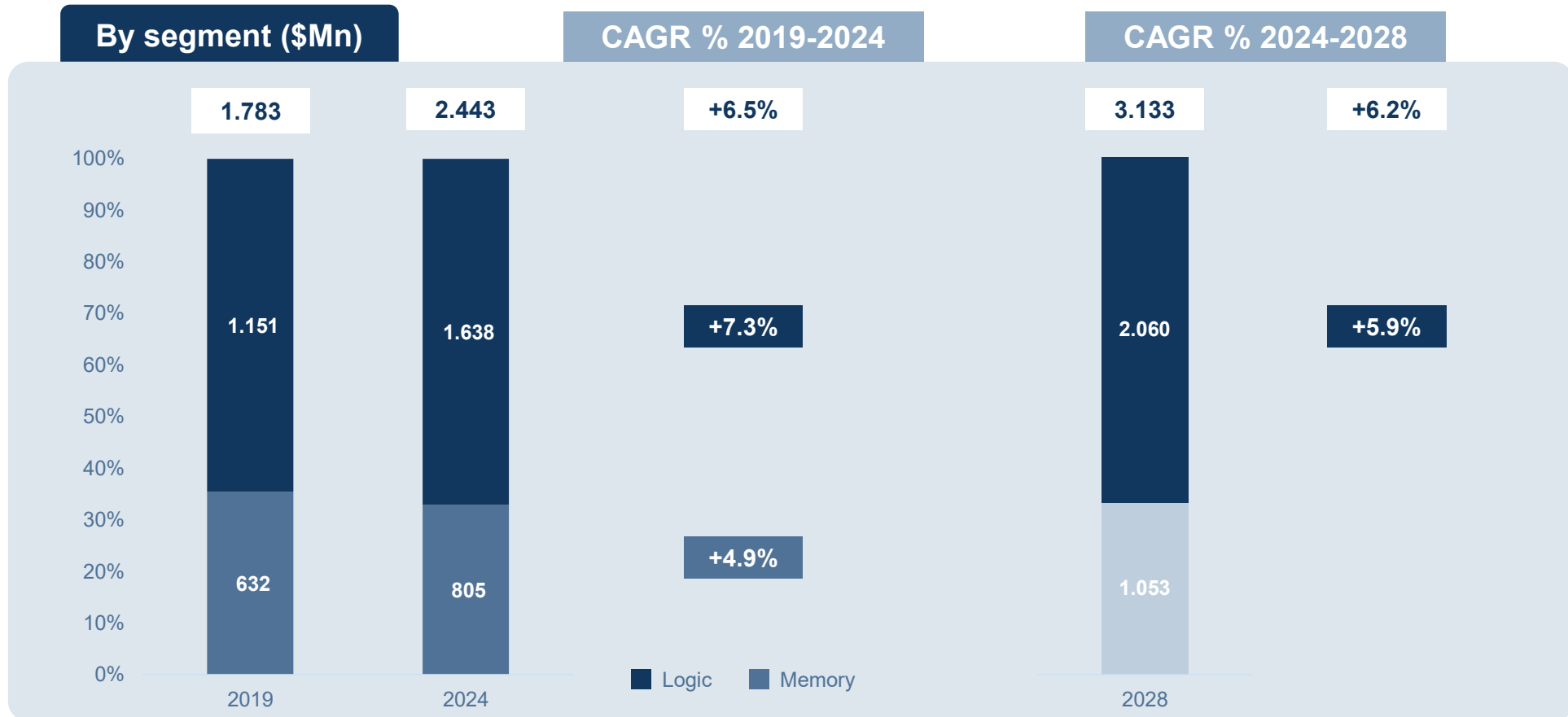
# Reference Market



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# Overview of the Semiconductor Probe Cards market

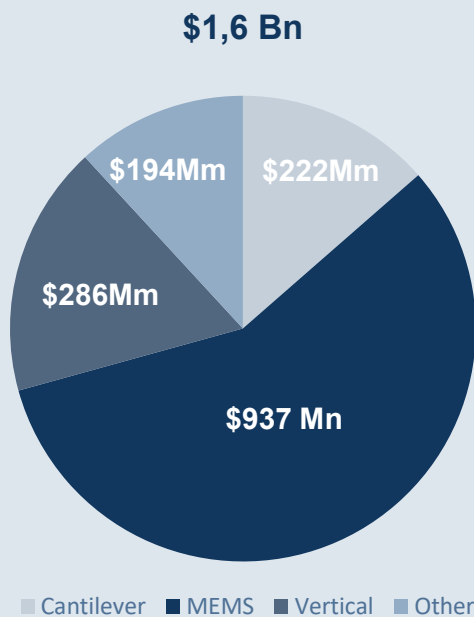


Source: Yole – Semiconductor Test Consumables market monitor Q3 2024 (Sept. 2024) – rounded figures. Memory: DRAM+NVM & Other memory. Logic: MEMS, Power, RF, CMOS Image Sensors, Photonics, Other non-memory, WAT.



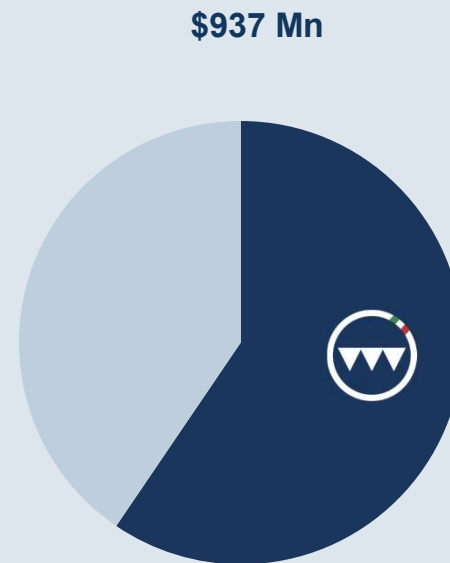
# Our reference market

2024 Logic Probe Card market



**Market Share: 34%**

2024 MEMS Logic Probe Card

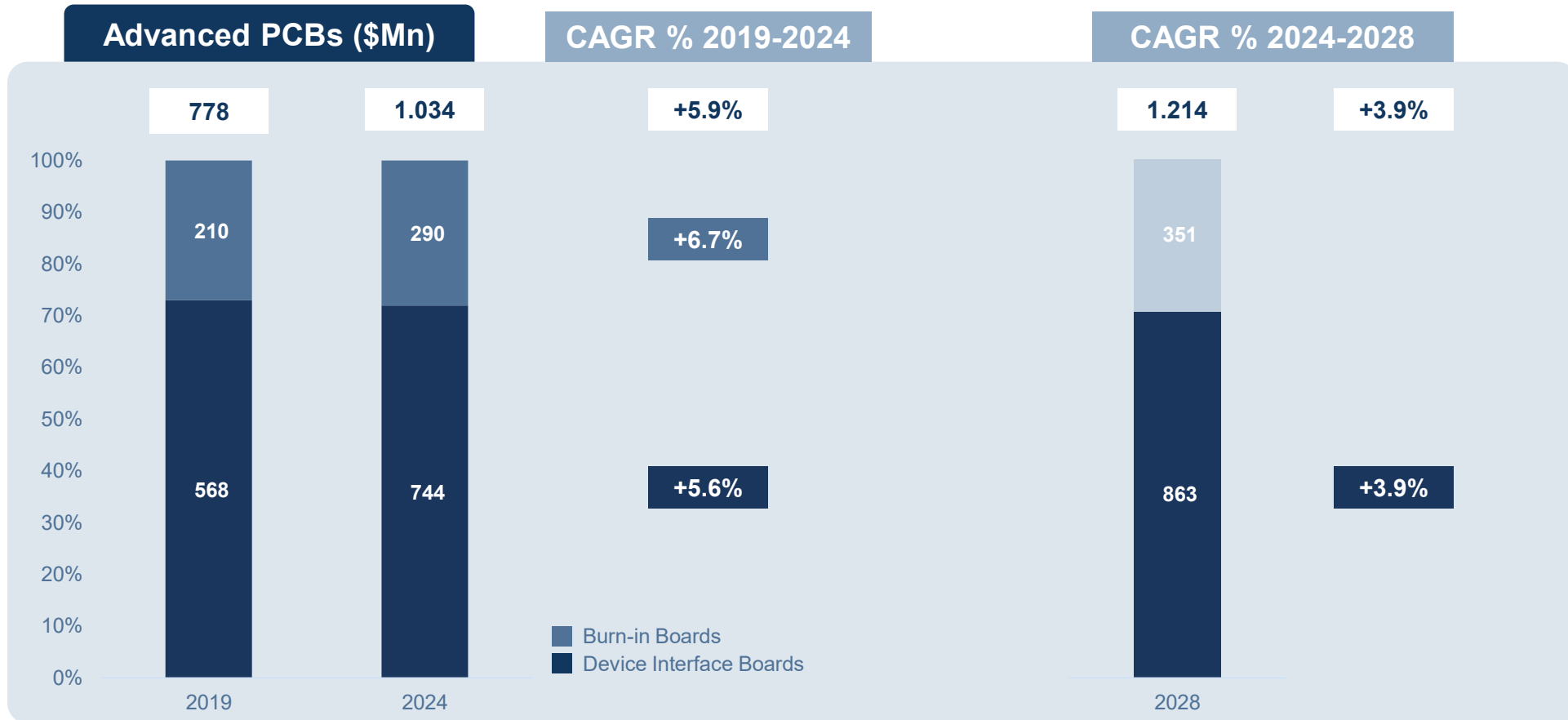


**Market Share: 60%**

Source: Yole – Semiconductor Test Consumables market monitor Q3 2024 (Sept. 2024) – rounded figures.



# Final Testing market – Advanced PCBs

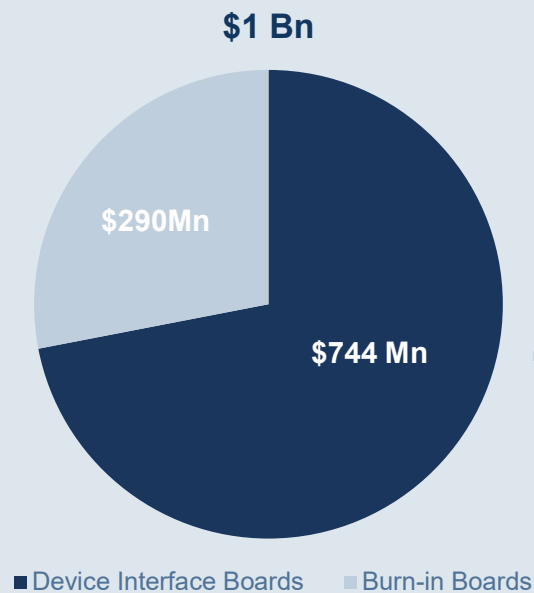


Source: Yole Test Interface Board market monitor Q3 2024 (Sept. 2024) – rounded figures.



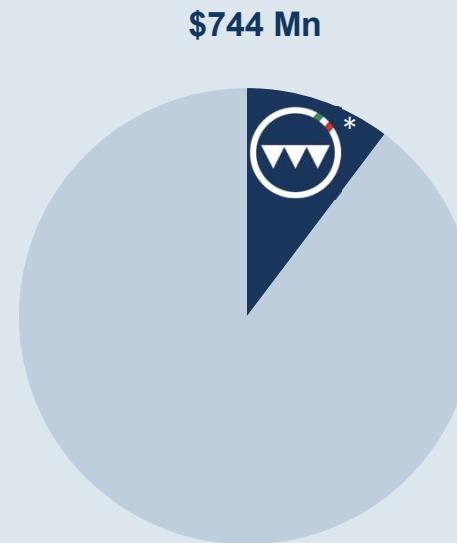
# Final Testing market – Our reference market

## 2024 Advanced PCB for semiconductor



**Market Share: 6%**

## 2024 Final Test DIB market



Source: Yole Test Interface Board market monitor Q3 2024 (Sept. 2024) – rounded figures.  
(\*) Based on DIS Tech Final Test FY24 data. Company acquired by Technoprobe on May 27, 2024.





# Business Model



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# A successful and vertically integrated business model





## Supported by an open eco-system partnerships

# TERADYNE

**Accelerate growth** of  
complete Probe Card and  
Final Test Interfaces by  
acquisition of DIS

**Joint Development Projects**  
to deliver superior customer  
value in SOC and Memory



# TECHNOPROBE

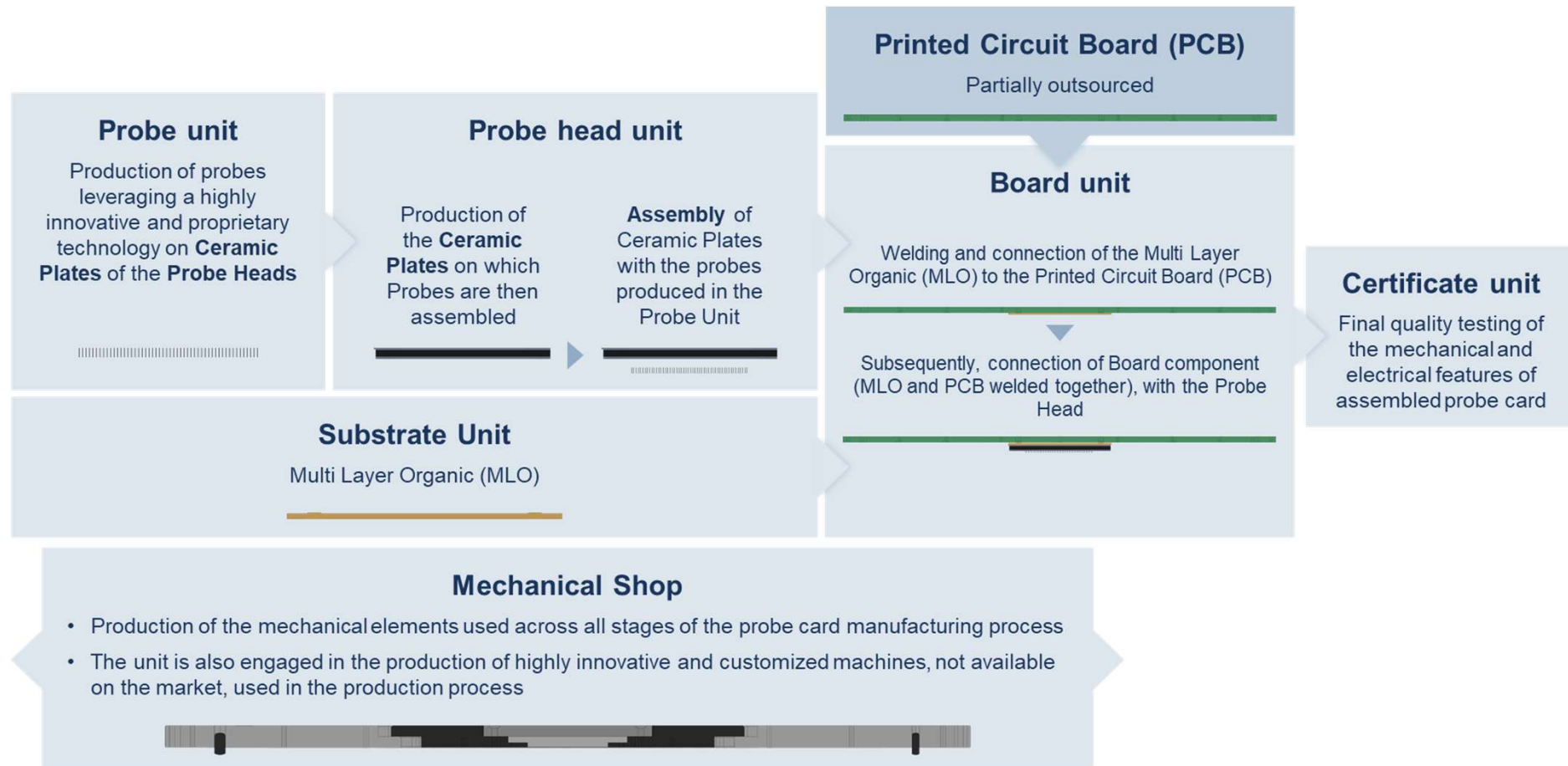
# ADVANTEST

**Priority suppliers**  
of PCB

**Joint Development Projects**  
to share knowledge



# The Probe Card manufacturing process



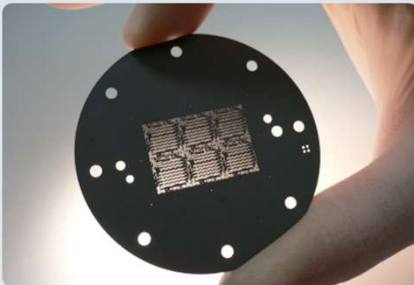




# The wide range of highly innovative technologies inside

## Advanced micromachining

Advanced laser cutting:  
high accuracy and fast lead time



## Thin film

Strong investment in advanced  
thin film technology to reduce  
lead time and improve quality  
and complexity



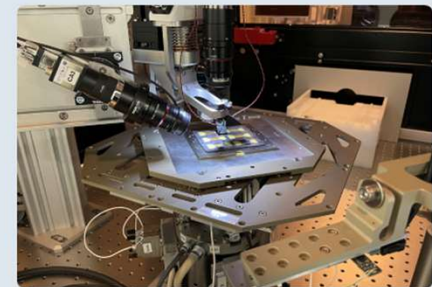
## 3D MEMS

Acquisition of MICROFABRICA  
in 2019; the sole company in the  
world specialized in 3D metallic  
MEMS manufacturing



## Advanced manufacturing

Advanced manufacturing for high  
volume and best quality  
assembly of micro components





# Vision & Strategy



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# Challenges & strategic setting

**1** **Evolution of chip technology**  
(more than Moore)  
Scaling slow down as enabler for **chiplets**,  
**3D architectures** and **new materials**

→ **Continuous investments in R&D**  
→ **M&A as accelerator of technological development**

**2** **Increase in complexity**  
**Design and manufacturing** are becoming essential capabilities to reliably deliver **complex solutions**

→ **Strategic partnerships**  
→ **Vertical integration of the most value-added components of the probe card**

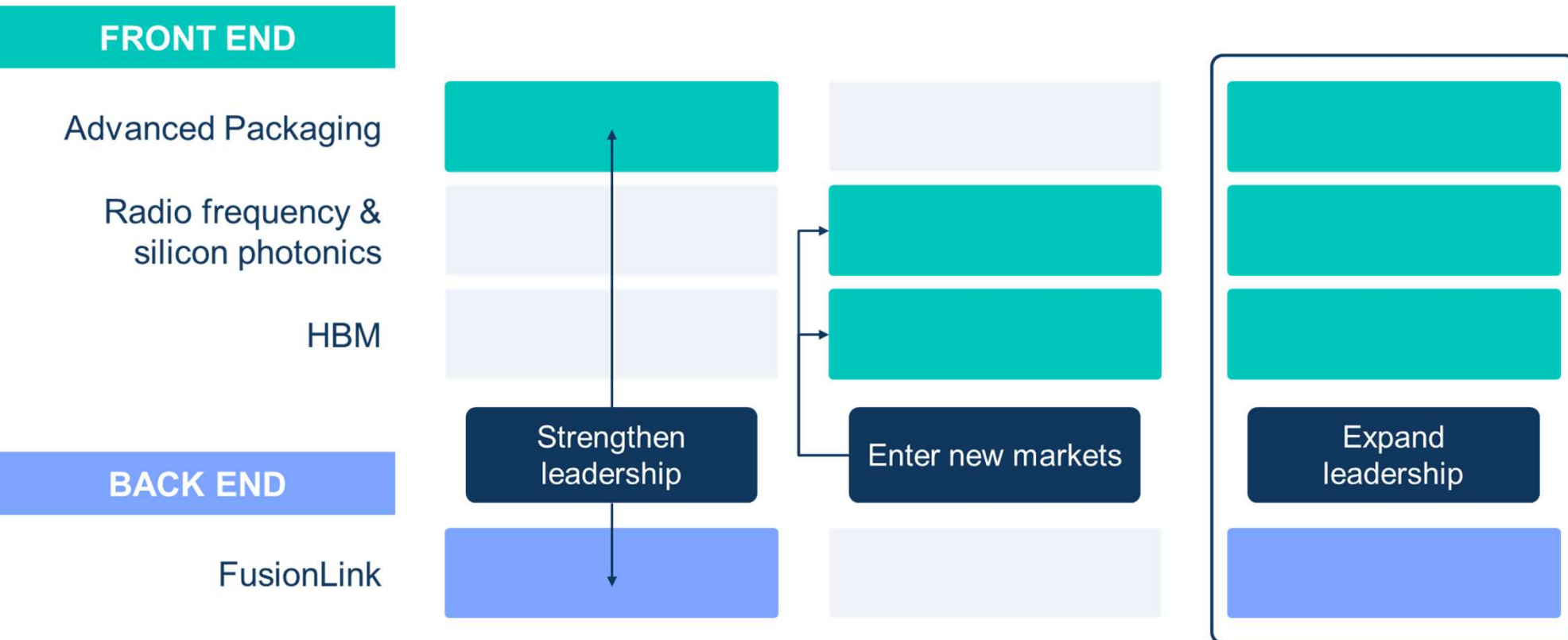
**3** **Client satisfaction**  
**Reliability** of the product & **on-time delivery**

→ **Support on site**  
→ **Commercial agreements**



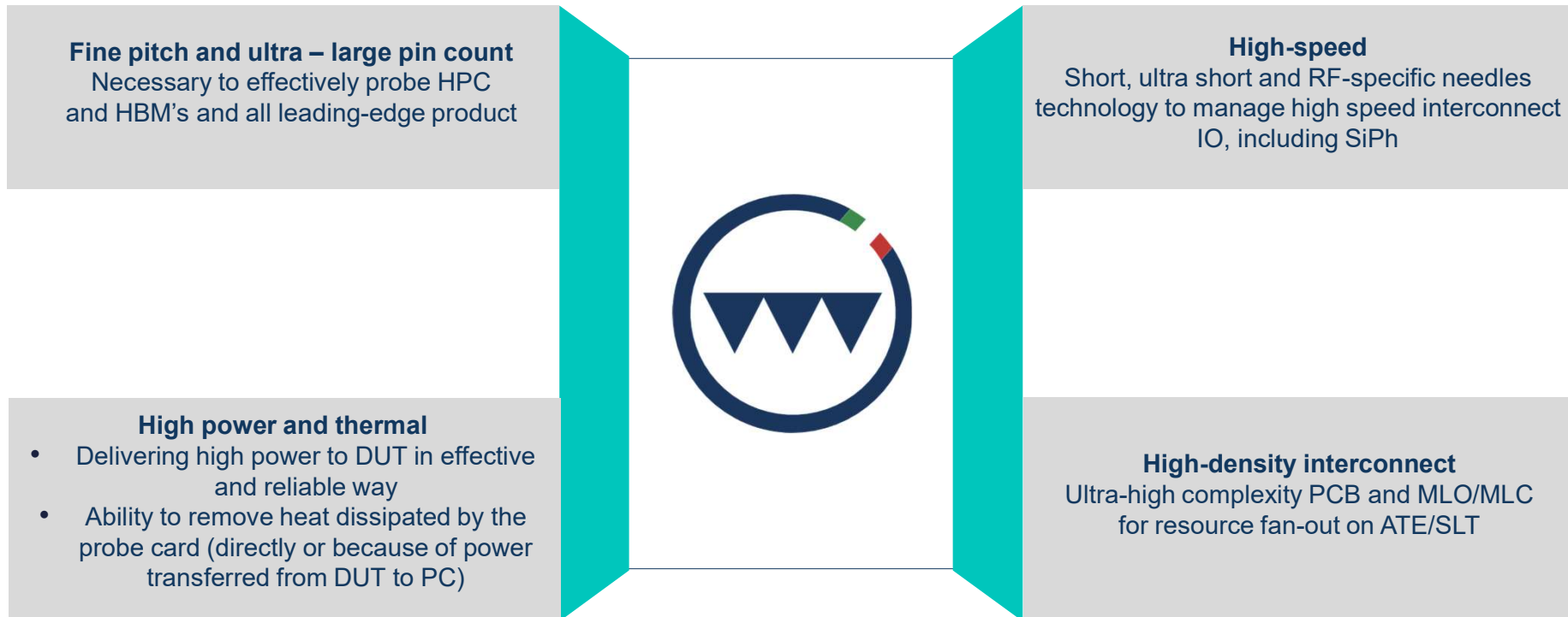


# Growth drivers & trajectories





# Technoprobe as advanced packaging enabler





# A hungry world of wideband applications



Exponential increase in number & type of connected things



Increasing reliance on the cloud



Bandwidth-hungry applications

## Analog radio frequency

Satellite communications and sensing, automotive radar, mobile communication,...



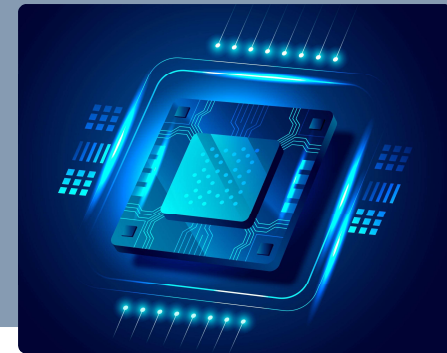
## Chiplet probing

High density and high-speed IO inside chiplet demand for high-performance probe needles



## Silicon photonics

Chiplet to chiplet interconnect / photonics-driven computing

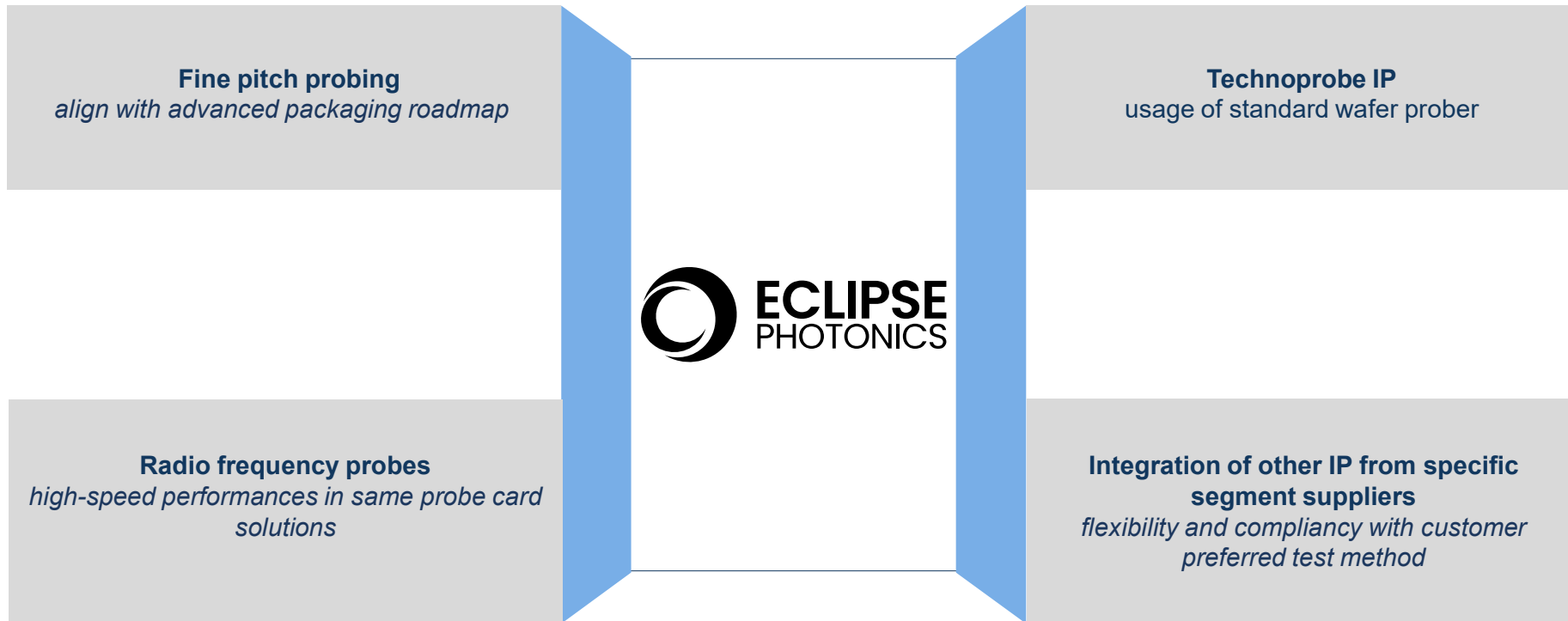


**FRONT END** Proliferate radio frequency and silicon photonics

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# Technoprobe silicon photonics testing solution



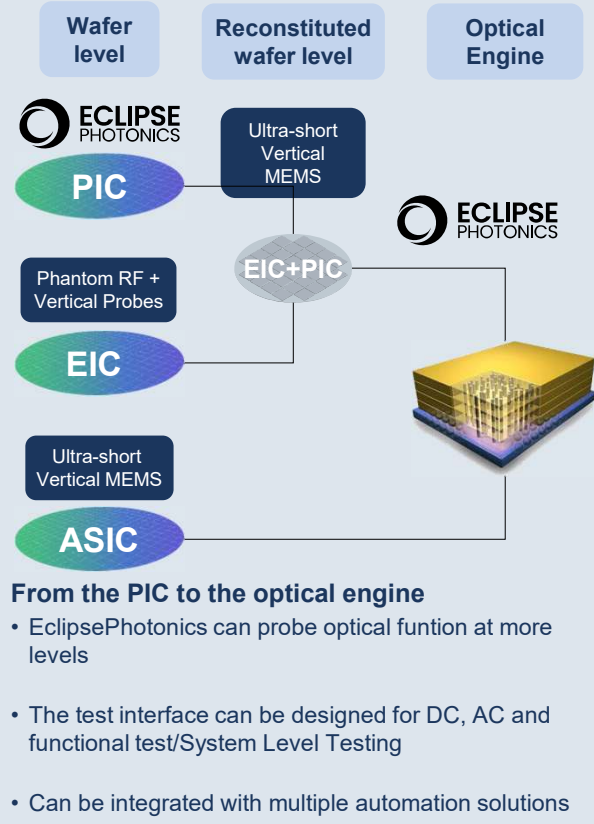
**FRONT END** Proliferate radio frequency and silicon photonics

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# Eclipse photonics

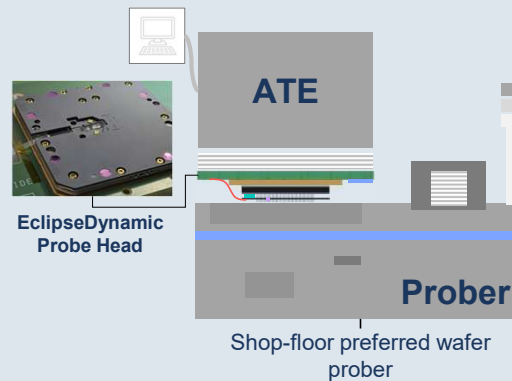
## Where it applies



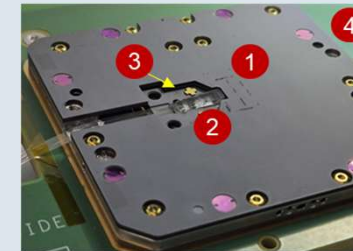
## How it works

### An autonomous instrument

- EclipsePhotonics embeds the electronics to autonomously operate when on the tester
- It integrates a programmable unit to execute the alignment algorithm(s), interface to the tester and operate the electronics
- The integration with ATE gives the capability to control the instrument from the user test program



## What it delivers



### Probe card content

- Vertical MEMS needle and Phantom RF probes
- FAU, fiber optics and optical connector (blind mated)
- FAU positioner (up to 6-axis)
- Electronics to activate and control the positioner

### What it delivers

- Direct docking
- Integrated optical and electrical probe, with off-line card certification
- High operation stability, repeatability and immunity to external factors
- In-field repairability
- Minimal optical to electrical pin distance constraints

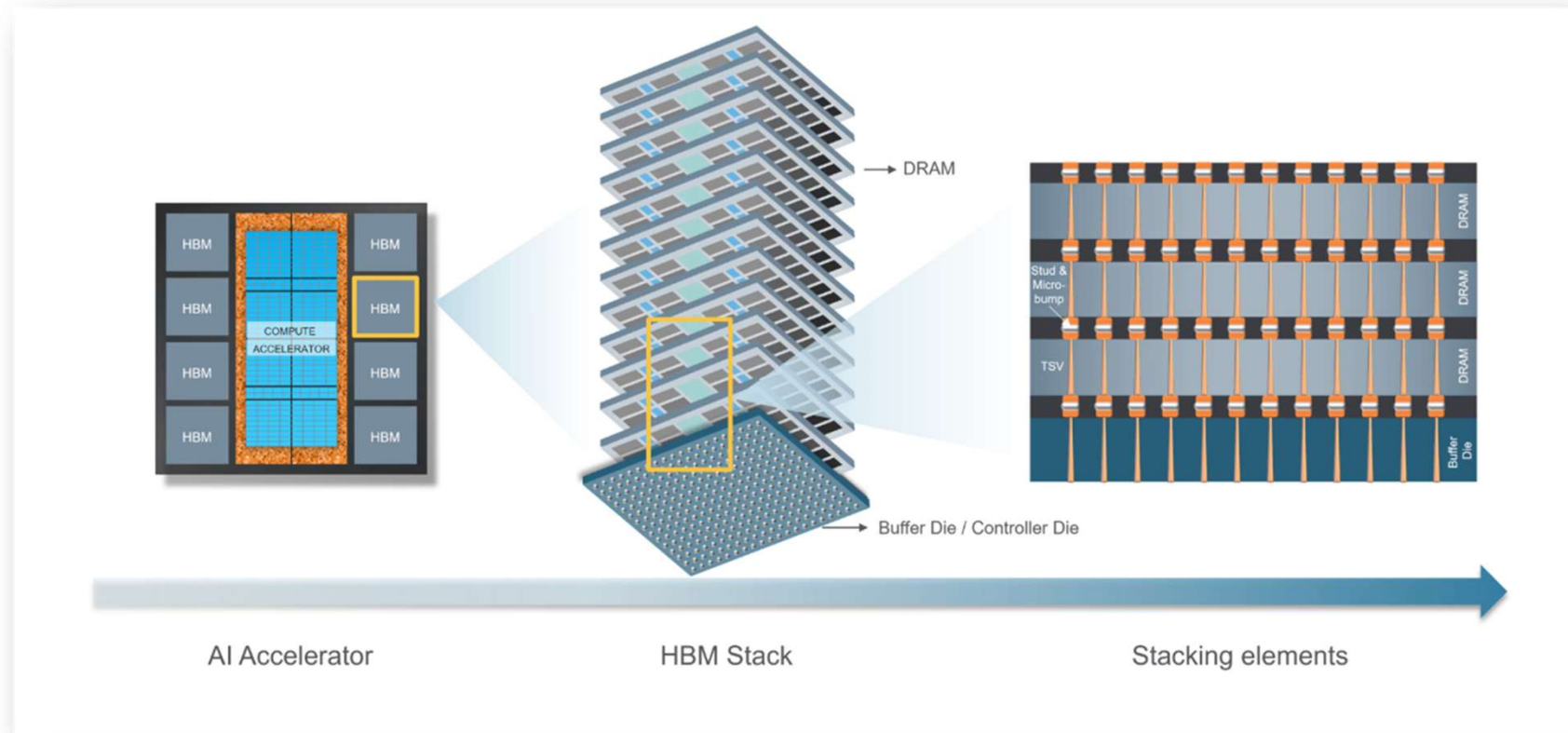
**PIC:** photonics integrated circuit **EIC:** electronic integrated circuit **ASIC:** Application-Specific Integrated Circuit

**FRONT END** Proliferate radio frequency and silicon photonics

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# HBM Architecture



Cartoon credit: Applied Material web site

**FRONT END** Enter the High Bandwidth Memory (HBM) segment

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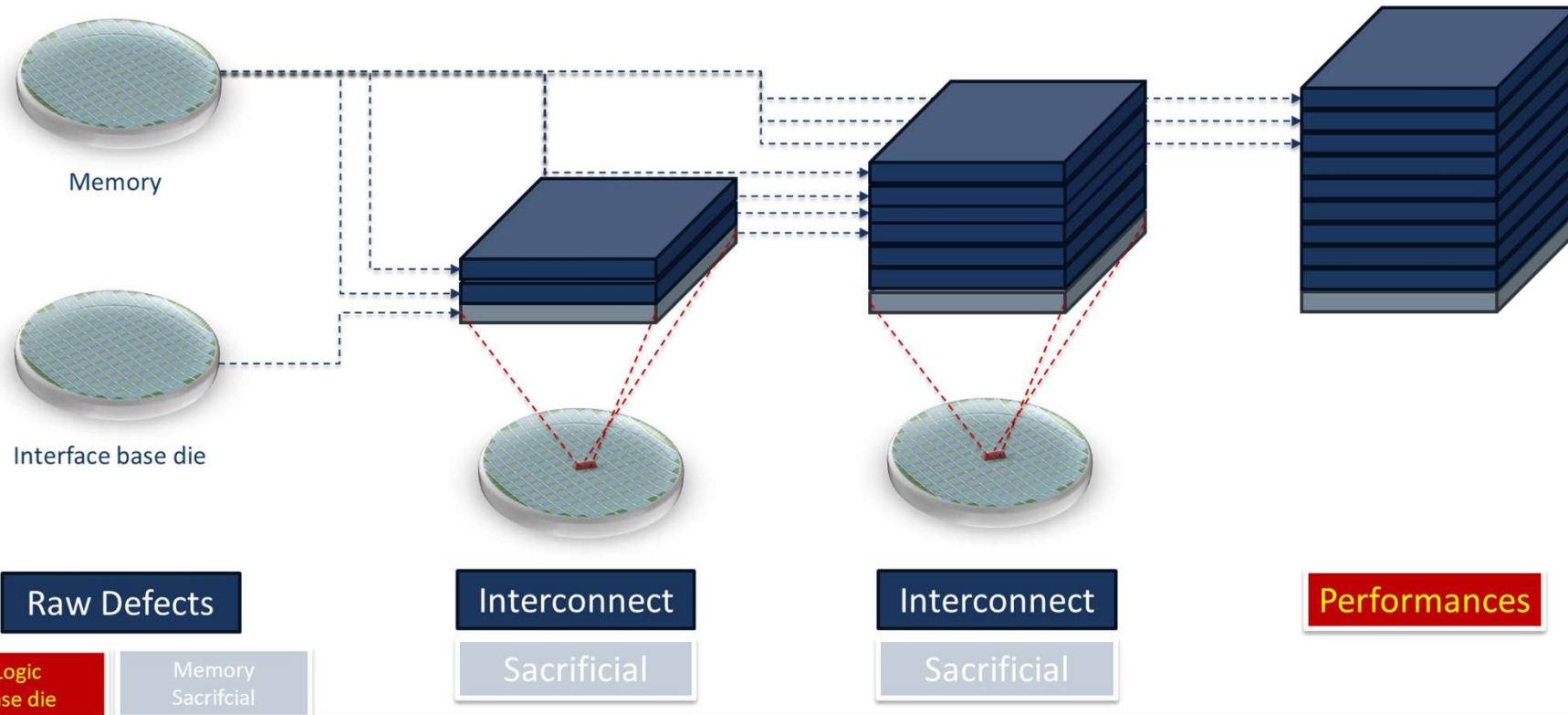


# HBM Test Flow

Wafer level

Intermediate ?  
Reconstituted wafer level

HBM cube  
Singulated Die level



FRONT END Enter the High Bandwidth Memory (HBM) segment

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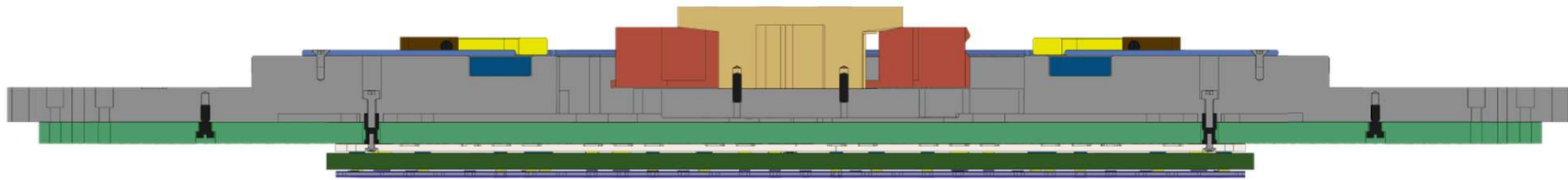


# HBM: new testing solution

DRAM and HBM are typically tested with **microcantilever** probing technologies.

Most **advanced HBM** and Next Generation products are becoming more challenging in terms of pad pitch, signal integrity, and power.

For both applications Technoprobe is leveraging on **Vertical MEMS** solution and on a unique PC architecture.



**FRONT END** Enter the High Bandwidth Memory (HBM) segment

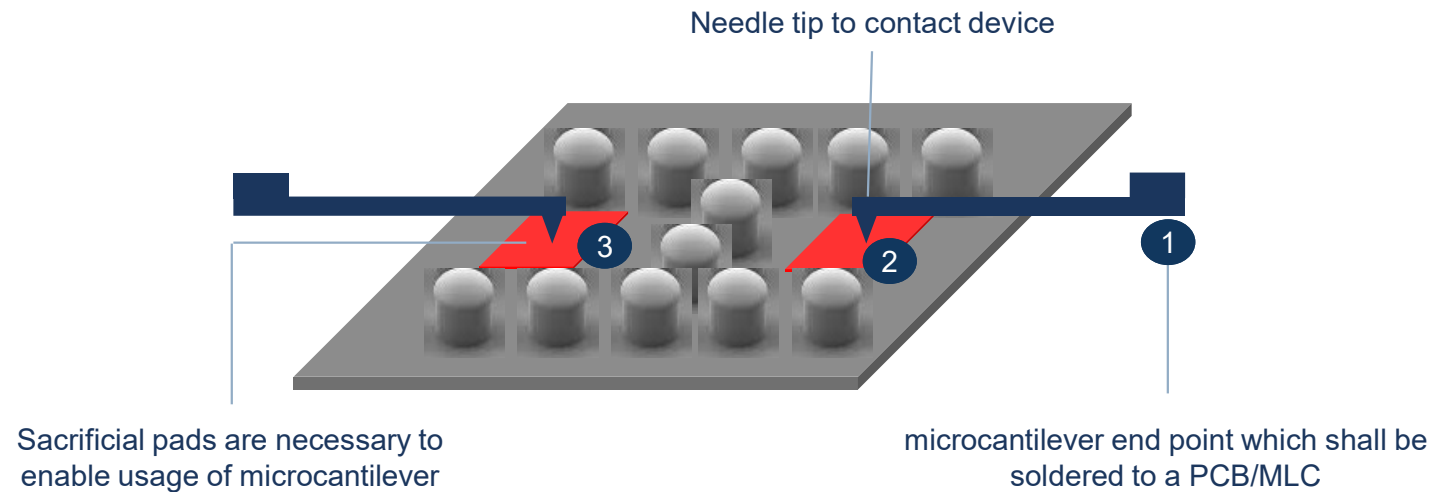
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# HBM Test Flow: microcantilever technology

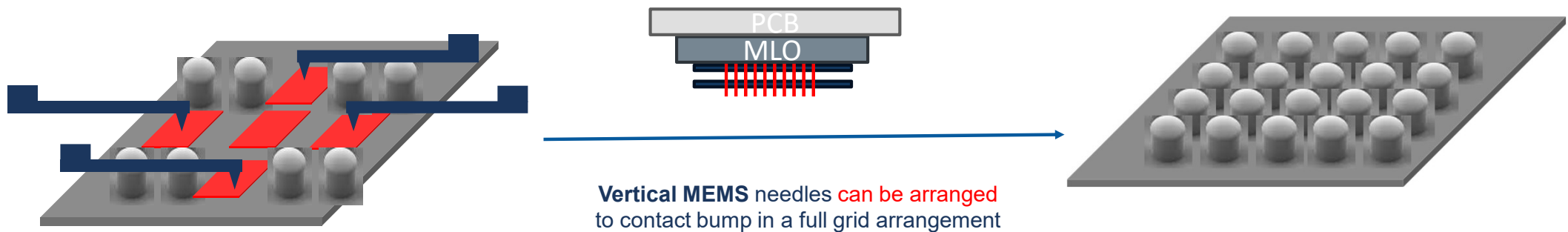
## Microcantilever

needles **cannot be** arranged to contact bump in a full grid arrangement





# HBM Test Flow: vertical mems vs. microcantilever



FRONT END Enter the High Bandwidth Memory (HBM) segment

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# FusionLink



**FusionLink is an advanced interface architecture that combines the best manufacturing technologies & processes to redefine what's possible for test strategy**

- FusionLink unifies the know-how across probe cards and device interface boards under one architectural framework
- FusionLink brings together the latest advances in semiconductor packaging and high-performance materials with Technoprobe's proprietary innovations in design, fabrication, assembly, and verification
- The architecture is not a "one size fits all" but is meant to be optimized per project



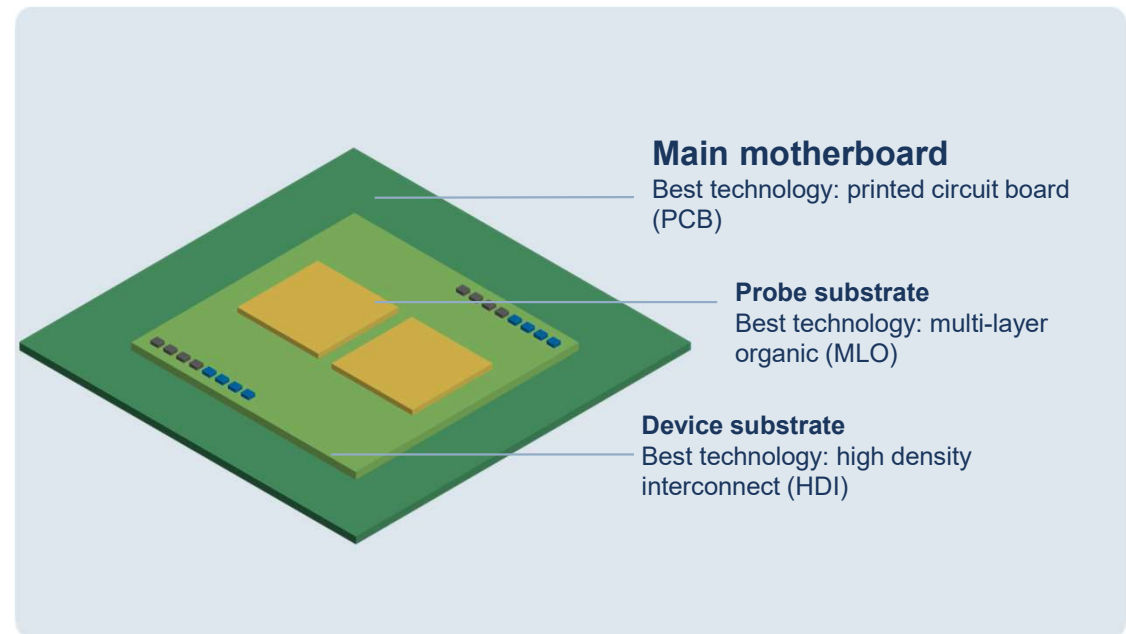
## The Best Performance



## The Highest Quality



## Faster Time to Market





# Financial Outlook



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# Mid-terms scenario

## 1 Technological complexity evolution

- Testing solution for Advanced Packaging
- Increase in demand for high-precision tests

## 2 Market trends

- AI will lead the growth for many market segments
- Expansion of memory semiconductor segments

## 3 Geo-political instability

- Technological sovereignty
- Commercial policies



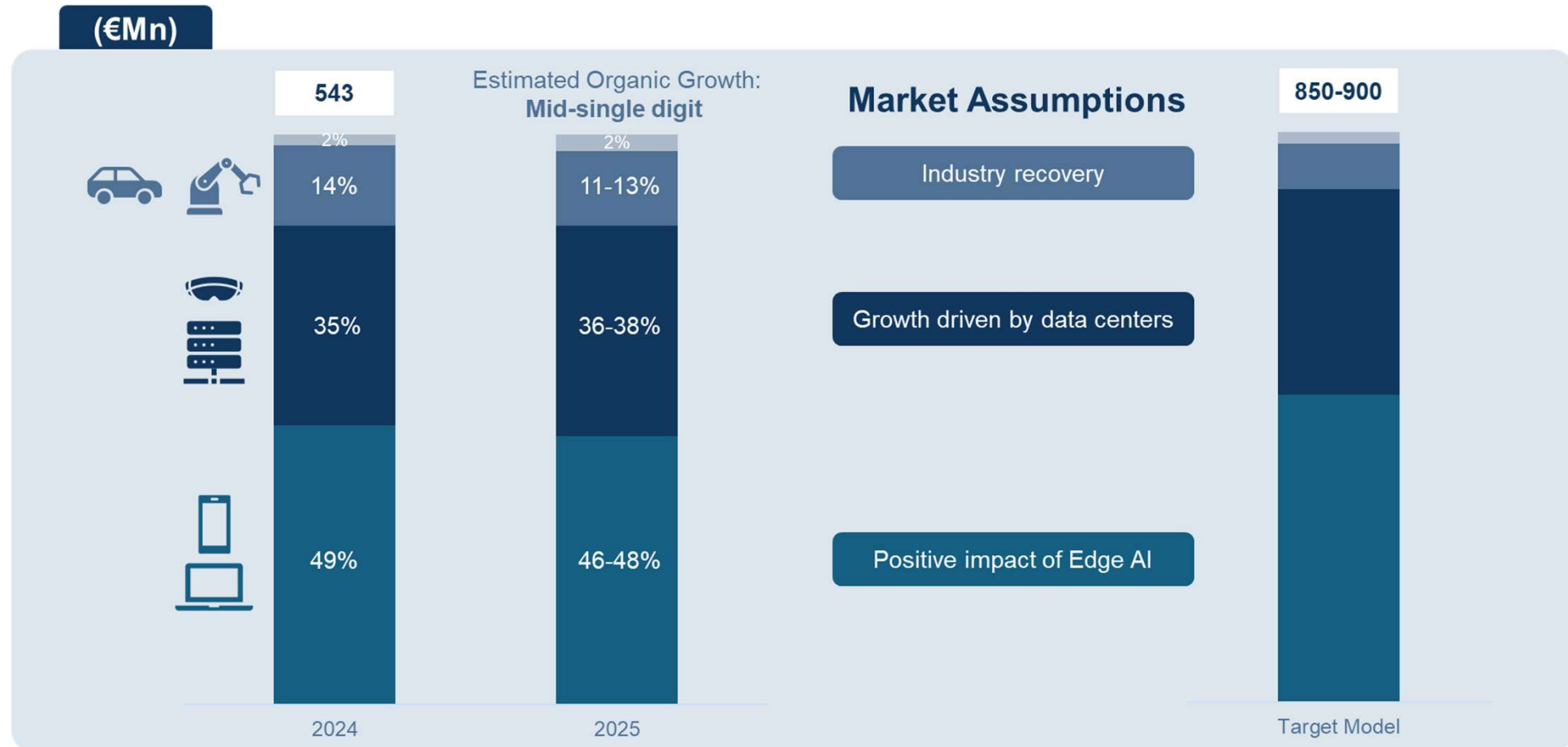
# Market trends & revenues path





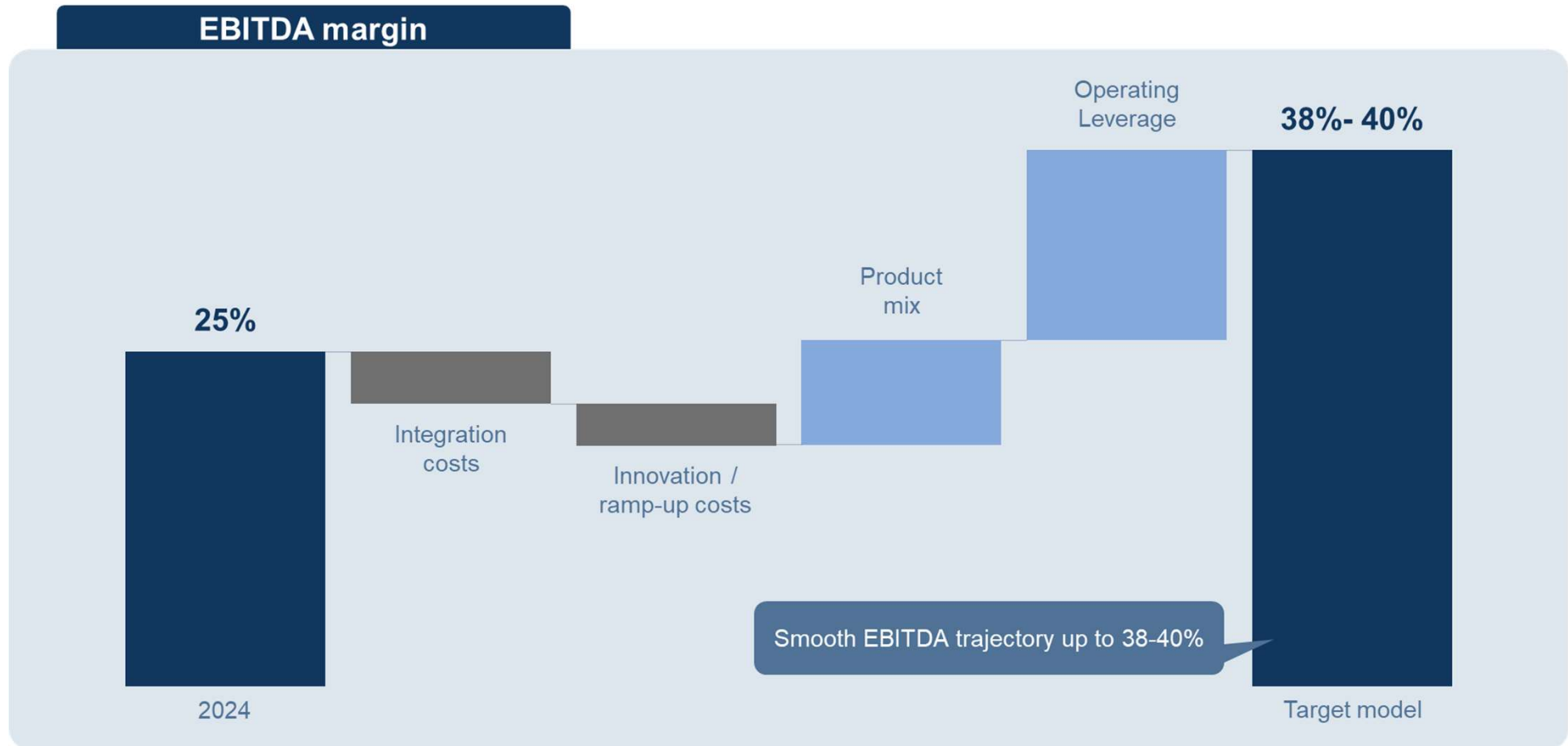


# Market trends & revenues path





# Profitability profile





## 9M 2025 market drivers



*Consistent growth in AI*



## Revenues at 466.6€m

down 16.6% QoQ  
up 20.6% YoY



*Slight increase in Consumer market*



*Softness in Automotive and Industrial*





# Financial Highlights

**Q3 2025**

**Revenues** were **140.7€m**

*down 3.5% YoY, down 16.6% QoQ*

**Gross Profit** was **56.7€m**

*down 4.6% YoY, with a margin of 40.3%*

**Ebitda** was **39.8€m**

*up 15.0% YoY, with a margin of 28.2%*

**9M 2025**

**Revenues** were **466.6€m**

*up 20.6% YoY*

**Gross Profit** was **207.3€m**

*up 29.5% YoY, with a margin of 44.4%*

**Ebitda** was **146.1€m**

*up 53.3% YoY, with a margin of 31.3%*



# 9M 2025 results

	9M 2025	9M 2024	YoY%	Notes
<b>Revenues (€m)</b>	<b>466.6</b>	<b>386.9</b>	<b>+20.6%</b>	<ul style="list-style-type: none"> <li>• <b>Organic growth:</b> rising trend in AI and slight increase in consumer, partially offset by shrinkage in auto and industrial</li> <li>• <b>Change in perimeter</b> (DIS contributed for 9 months in 2025 vs 4 months in 2024)</li> <li>• <b>FX negative impact</b> for €12m</li> </ul>
<b>Gross Profit (€m)</b>	<b>207.3</b>	<b>160.1</b>	<b>+29.5%</b>	<ul style="list-style-type: none"> <li>• <b>Recovering in production efficiency</b></li> <li>• <b>Operating leverage</b></li> </ul>
<i>% margin</i>	<i>44.4%</i>	<i>41.4%</i>	<i>+300 bps</i>	
<b>Ebitda (€m)</b>	<b>146.1</b>	<b>95.3</b>	<b>+53.3%</b>	<ul style="list-style-type: none"> <li>• <b>Ebitda margin benefited</b>, in addition to the above, also from US reorganization positive impact, terminated in H1 2025</li> </ul>
<i>% margin</i>	<i>31.3%</i>	<i>24.6%</i>	<i>+670 bps</i>	
	<b>9.30.2025</b>	<b>12.31.2024</b>		
<b>Net Financial Position (€m)</b>	<b>665.7</b>	<b>656.3</b>		<b>Variance mainly</b> attributable to solid <b>cash flow from operating</b> activities (+114€m) and the disposal of Santa Clara building (+26€m), partially offset by <b>Capex</b> (-51€m), the acquisition of a <b>minority stake in Yee Wei Inc.</b> (-20€m) and <b>Innostar Service Inc.</b> (-7€m), together with <b>shares buy back program</b> (-32€m) and <b>the unrealized fx impact</b> on foreign currency bank accounts (-23€m)



# Q4 2025 Guidance

**Revenues: 160€m**

(+/-3%)

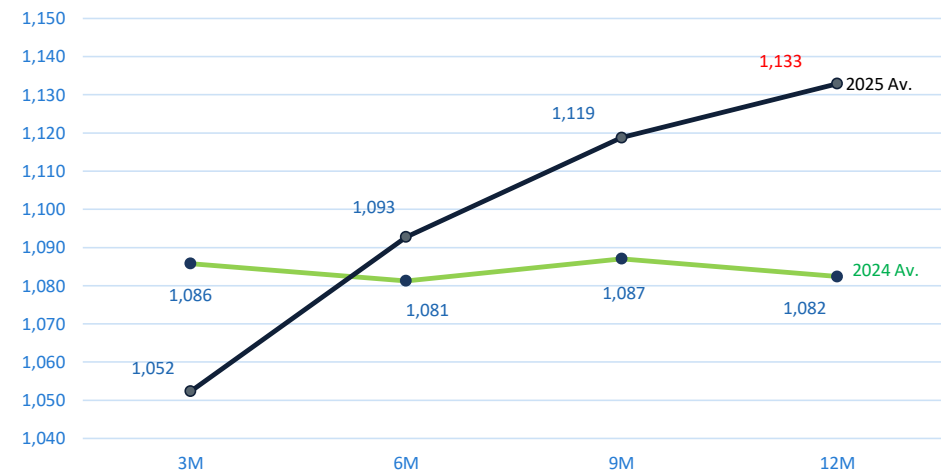
**Gross Margin: 46%**

(+/-200bps)

**Ebitda Margin: 34.7%**

(+/-200 bps)

EUR/USD - Accumulated Average by Quarter



Average	Q1 '24	Q2 '24	Q3 '24	Q4 '24	Q1 '25	Q2 '25	Q3 '25	Q4 '25*
	1,086	1,077	1,098	1,068	1,052	1,134	1,168	1,175
3M	1,086				1,052			
6M	1,081				1,093			
9M		1,087			1,119			
12M			1,082			1,133		

\*Estimate